singulation, the dies are tested while still a part of the wafer. Die selector circuits are also formed in the wafer between the dies. The die selector circuits are used to select desired ones of the dies for testing. The die selector circuits have two or four clock signals interconnected with adjacent die selector circuits. The sequence of clock signals specifies the die or dies to be selected for testing. The interconnection of two or four clock signals facilitates testing even if the interconnection of one of more clock signals between die selector circuits is broken or opened.

In the Claims:

Cancel claims 3-19 and 30-34.

Remarks

Applicant thanks the examiner for the explanation of the rejections of this application.

Applicant confirms the election of claims 20-29 without traverse.

The new Abstract complies with the existing requirements.

Claims 20 through 29 find support in the present application. Applicant re-states these claims with figure numbers and reference numerals to identify the specific matters in the drawings that support, but do not limit, the terms of the claims.